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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/926,454	11/06/2001	Syouji Higashida	107400-00044	4669

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EXAMINER	
MONDT, JOHANNES P	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/926,454	HIGASHIDA ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-6,8 and 9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-6,8 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed June 30, 2004 forms the basis for this official action. In said Amendment Applicants substantially amended claims 8 and 9, and thereby substantially amended all pending claims 2-6 and 8-9. Claims 1 and 7 are canceled. Comments on Remarks in said Amendment are included below under "Response to Arguments".

Response to Arguments

Applicants' arguments in traverse have been fully considered but are not deemed persuasive:

In particular, although Yamamoto et al does not appear to verbally teach complete closure of both Zener diode p-type and n-type layers *and* outer gate metal film attached thereto, Yamamoto et al do teach encirclement of the cell region by the Zener diode 9 while the source metal film clearly is on the inside (in cell region 10). However, a more explicit teaching can be found in Frisina (5,886,381) replacing Yamamoto et al as the secondary reference.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claim 8 and 2-6*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al (6,268,242 B1) in view of Frisina (5,886,381).

On claim 8 (which is the independent claim): Williams et al teach a semiconductor device (cf. title) comprising:

an insulating gate field effect transistor comprising a plurality of transistor cells (separated by a width W; see Figure 1) which are arranged in a semiconductor layer 108 (cf. column 3, lines 39-40) and connected in parallel; and a protective diode D1 (and D2) (cf. column 3, lines 58-64) connected between a gate and a source of said insulating gate field effect transistor to prevent break-down due to a voltage greater than or equal to a particular value (cf. col. 7, l. 14-34) (furthermore, the limitation "to prevent.." above is functional language and in any case would not add any patentability to the claim in the present device application), wherein said protective diode is formed as a bi-directional diode in which one or more ring-shaped p-type layers and one or more ring-shaped n-type layers 130 (cf. column 3, lines 58-64) are flatly and alternately provided on an insulating layer 132 (cf. column 3, line 60) at a peripheral portion of a region of said transistor cells, a source wiring 112 (cf. column 3, line 62) (cf. Figures 7A and 7B) contacts with the innermost layer of said protective diode, and a metal film 134, said metal film being ring-shaped (that the ring is open is a different matter, covered by the remainder of the claim language (final two lines of claim) and addressed below in connexion with the relevant claim language), contacts with the outermost layer of said protective

diode (cf. col. 3, l. 58-63), said metal film 134 being successively formed with a gate electrode pad 710 comprising a metal film (cf. col. 3, l. 58-63, Figure 7B).

Williams does not necessarily teach (a) the one or more ring-shaped p-type layers and ring-shaped n-type layers to be *closed*, nor (b) that metal film 134 be a closed ring-shaped metal film substantially contacting the full circumferential length of the outermost layer. However, it would have been obvious to improve the invention by Williams to include (a) *closed* ring-shaped p-type layers, n-type layers and (b) to select a *closed* ring-shaped metal film substantially contacting the full circumferential length of the most outer layer in view of Frisina, who teaches for the specific purpose of increasing the junction surface area, and thereby inherently increasing the electrostatic strength, that said Zener diode, and hence its contact metal (without contact metal on both sides of said Zener diode said Zener diode would not function as protection diode between source metal region and gate metal region (see abstract of Frisina) be formed so as to extend along the *whole perimeter* of the integrated insulated gate field effect device (title and abstract, particular its final sentence, Figure 4 showing Zener diode 11, gate metal region 44 (col. 4, l. 42), source metal region (col. 3, l. 58-59); and col. 2, l. 18-44; see plan view of Figure 4 represented by Figure 3, with Zener diode, and hence also p-type and n-type layers contained in 11 to be closed, and with outer ring-shaped gate metal film 44 completely closed).

Motivation to include the teaching in this regard by Frisina in the invention by Williams is the consequent improvement of the capability of the Zener diode to

protect against electrostatic discharge through. The inventions can be *combined* in this regard, because the contact area between the inner – and outermost Zener diode p-type or n-type layers with the metal films can easily be extended to form a Zener diode protection ring, as evidenced by the plan view of the invention by Williams (see Figure 7B). *Success* of the implementation of this combination can therefore be *reasonably expected*.

On claim 2: said ring-shaped metal film in Williams provided so as to contact with said outermost layer is a gate wiring successively formed with said gate electrode pad 710 (cf. Figure 7B).

On claim 3: the one ring-shaped metal film as essentially taught in the above-defined combination of the inventions by Williams et al and Frisina is a gate wiring 712 which has gate connecting portions so as to connect to gate electrodes of said transistor cells with partial striding over said protective diode in polysilicon layer 706 (cf. Figure 7A and column 10, line 1), and said gate connecting portions and source connecting portions of said source wiring which are contacted with said most inner layer are alternately formed in plan view (cf. Figure 7B).

On claim 4: the p-type and n-type layers in the above-defined combination of the inventions by Williams et al and Frisina made of polysilicon (cf. column 3, lines 58-63 and column 9, line 67 – column 10, line 1).

On claim 5: although neither Williams et al nor Frisina necessarily teach the further limitation as defined by claim 5, it is understood in the art of

semiconductor devices that the subsequent portions of the same conductivity type in the Zener diode, when having roughly the same width and the same impurity concentration, have approximately the same electrostatic breakdown properties so that the electrostatic load be about evenly divided, which is a reasonable choice. However, there is no compelling reason, why the above-mentioned ranges for the ratio of (a) width (around 1) and (b) impurity concentrations (around 1) is critical to the invention of Applicant, nor does Applicant show such criticality. Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

On claim 6: the semiconductor device as taught by Williams et al in view of Frisina has a diffusion region of P+ conductivity type formed on the closest side to said protective diode of said transistor cells arranged (therein), namely the P+ region abutting region 100A (cf. column 3, line 50 and column 3, lines 35-48) in Figure 1, and said source wiring 112 contacting the innermost layer of said protective diode is contacted (is in direct contact) with said P+ region (see Figure 1). It is observed that said P+ region has no other diffusion region therein: abutting N+ region is a separate diffusion region next to it.

2. ***Claim 9*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams et al (6,268,242 B1) in view of Frisina (5,886,381) and Throngnumchai et al (4,963,970). Williams et al teach a semiconductor device (cf. title) comprising:

an insulating gate field effect transistor comprising a plurality of transistor cells (separated by a width W; see Figure 1) which are arranged in a semiconductor layer 108 (cf. column 3, lines 39-40) and connected in parallel; and

a protective diode D1 (and D2) (cf. column 3, lines 58-64) connected between a gate and a source of said insulating gate field effect transistor to break down an input of a constant voltage or more applied between said gate and said source (inherent in diode),

wherein said protective diode is formed as a bi-directional diode in which one or more ring-shaped p-type layers and one or more ring-shaped n-type layers 130 (cf. column 3, lines 58-64) are alternately provided on an insulating layer 132 (cf. column 3, line 60) at a peripheral portion of a region of said transistor cells, said protective diode having three or more layers (cf. Figures 1 and 3 in addition to Figure 7B), a source wiring 112 (cf. column 3, line 62) (cf. Figures 7A and 7B) contacts with one layer of said protective diode, and a metal film 134 contacts with another layer of said protective diode (cf. col. 3, l. 58-63), said metal film 134 being successively formed with a gate electrode pad comprising a metal film (cf. col. 3, l. 58-63, Figure 7B) and being ring-shaped (cf. Figure 7B; that the ring is open is another matter, covered by the final sentence of the claim and addressed below in the rejection with regard to it), said one

and other layers being positioned at the ends of said protective diode, but arranged in a horizontal direction.

Williams does not necessarily teach (a) the one or more ring-shaped p-type layers and ring-shaped n-type layers to be *closed*, nor (b) that metal film 134 be a closed ring-shaped metal film substantially contacting the full circumferential length of the outermost layer. However, it would have been obvious to improve the invention by Williams to include (a) *closed* ring-shaped p-type layers, n-type layers and (b) to select a *closed* ring-shaped metal film substantially contacting the full circumferential length of the most outer layer in view of Frisina, who teaches for the specific purpose of increasing the junction surface area, and thereby inherently increasing the electrostatic strength, that said Zener diode, and hence its contact metal (without contact metal on both sides of said Zener diode said Zener diode would not function as protection diode between source metal region and gate metal region (see abstract of Frisina) be formed so as to extend along the *whole perimeter* of the integrated insulated gate field effect device (title and abstract, particular its final sentence, Figure 4 showing Zener diode 11, gate metal region 44 (col. 4, l. 42), source metal region (col. 3, l. 58-59); and col. 2, l. 18-44; see plan view of Figure 4 represented by Figure 3, with Zener diode, and hence also p-type and n-type layers contained in 11 to be closed, and with outer ring-shaped gate metal film 44 completely closed).

Motivation to include the teaching in this regard by Frisina in the invention by Williams is the consequent improvement of the capability of the Zener diode to protect against electrostatic discharge through. The inventions can be *combined* in this regard,

because the contact area between the inner – and outermost Zener diode p-type or n-type layers with the metal films can easily be extended to form a Zener diode protection ring, as evidenced by the plan view of the invention by Williams (see Figure 7B). *Success* of the implementation of this combination can therefore be *reasonably expected*.

Conclusion

2. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
September 21, 2004

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